

CS-01-214



December 12, 2003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/662,674 09/15/03 |

Yong Meng Lee et al.

METHOD OF FORMING DOUBLE-GATED
SILICON-ON-SILICON (SOI) TRANSISTORS
WITH CORNER ROUNDING
| _____ |

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 12/19/03

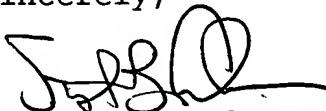
U.S. Patent 6,451,656 to Yu et al., "CMOS Inverter Configured from Double Gate MOSFET and Method of Fabricating Same," describes a double-gated transistor in semiconductor-on-insulator (SOI).

U.S. Patent 6,413,802 to Hu et al., "FinFET Transistor Structures Having a Double Gate Channel Extending Vertically From a Substrate and Methods of Manufacture," describes a double-gated FinFET on semiconductor-on-insulator (SOI).

U.S. Patent 6,365,465 to Chan et al., "Self-Aligned Double-Gate MOSFET by Selective Epitaxy and Silicon Wafer Bonding Techniques," describes a process for a double-gated MOSFET on semiconductor-on-insulator (SOI).

U.S. Patent 6,396,108 to Krivokapic et al., "Self-Aligned Double Gate Silicon-On-Insulator (SOI) Device," describes a process for a double-gated MOSFET on semiconductor-on-insulator (SOI).

Sincerely,


Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

Document Number (Continued)

CS-01-214

Application Number

10/662,674

Applicant

Yang Meng Lee et al.

Filing Date

09/15/03

Group Art Unit

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

(Use several sheets if necessary)

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILED DATE IF APPROPRIATE
	6451656	9/17/02	Yu et al.	438	283	2/28/01
	6413802	7/2/02	Hu et al.	438	151	10/23/00
	6365465	4/2/02	Chan et al.	438	283	3/19/99
	6396108	5/28/02	Krivokapic et al.	257	365	11/13/00

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.